Nextest Magnum PV Tester

Manufacturer:	Nextest
Model:	Magnum PV
Location:	Asia
Quantity:	4
Inspectability:	Yes, can be inspected
Configuration:	

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System 4 Page 124-156

System 1

HOST

```
The test program is loading.
The test program is loaded.

Site 1 is the first site in Chassis 1
Site 4 is the last site in Chassis 1
  ui_SiteMask.........: 0xf
  ui_LoadedMask.......: 0xf
  ui_LoadedSlotMask..: 0xf
  ui_LoadedHOBSlotMask..: 0x0
HostName: XXXXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
ui_TestStarted: Cleared 0 test-done signals.
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
```

Site1_1_1

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXX
Nextest software release: C:\nextest\h3.9.5A
chassis 1 SET DB_DIAGCMD=1 -> success
```

TestStarted(1)...

Started: 08/23/18 17:23:07
Current Time is: 08/23/18 17:23:10

- Site controller details -
Intel(R) Pentium(R) III CPU - S 1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633

- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXX ***

Site 1 (Chassis 1, Slot 1)

Board Name	Serial Number	PWB Number	PWB Rev	PWA Number	PWA Rev	LVM SDR/DDR	DBM MBits	ECR1 MBits	ECR2 MBits	X bits	Y bits	D bits
HSB	822785	503539	2	503540	9	4/8	(2) 288 (2)	288 (2)	288 (2)	18*	16*	36*
PE_1	904889	503541	2	503542	3							
PE_2	905543	503541	2	503542	3							
PE_3	904938	503541	2	503542	3							
PE_4	902218	503541	2	503542	3							
DP_1	905315	504582	4	504583	15							
DP_2	901063	504582	3	504583	15							
DP_3	903577	504582	4	504583	15							
DP_4	902870	504582	4	504583	15							
IPC	916725	505306	5	505305	16	Firmware Revision : 3.6.2						

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	507322	505941	1		144	
DBM-DIMM2	507322	505941	1		144	
ECR1-DIMM1	505479	505935	1			144
ECR1-DIMM2	505479	505935	1			144
ECR2-DIMM1	505479	505935	1			144
ECR2-DIMM2	505479	505935	1			144
LVM1-DIMM1	505478	505947	1	4		
LVM2-DIMM1	505478	505947	1	4		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x9
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f


```
  ECR1 Fpga      0x1    0xc6
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM_X20 system# XXXXX
HOST computer name: XXXXX
N5VBB: -3.942
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
```


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Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
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Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
```


```
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
```


```
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
```


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  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
```


```
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
```

Site1_1_1V5M_Measure

V5M_Measure	Chassis_1	Slot_1						
V5M_Measure At: 08/23/18 17:23:11 On PEs: 904889 905543 904938 902218 and DPs: 905315 901063 903577 902870								
HostName	XXXXXXXX	HSB	822785					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.946	-5.4	-3.946	1.454	-0.15	0.15
Board_1	ADC_2	0	-3.941	-5.4	-3.941	1.459	-0.15	0.15
Board_2	ADC_1	0	-3.948	-5.4	-3.948	1.452	-0.15	0.15
Board_2	ADC_2	0	-3.938	-5.4	-3.938	1.463	-0.15	0.15
Board_3	ADC_1	0	-3.943	-5.4	-3.943	1.457	-0.15	0.15
Board_3	ADC_2	0	-3.932	-5.4	-3.932	1.469	-0.15	0.15
Board_4	ADC_1	0	-3.948	-5.4	-3.948	1.453	-0.15	0.15
Board_4	ADC_2	0	-3.94	-5.4	-3.94	1.461	-0.15	0.15

Site2_1_2

```
HSB1 SERIAL# XXXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/23/18 17:23:07
Current Time is: 08/23/18 17:23:10

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXX ***

                                                Site 2  ( Chassis 1, Slot 2 )
  Board         Serial    PWB      PWB   PWA      PWA       LVM        DBM       ECR1       ECR2       X      Y      D
  Name          Number    Number   Rev   Number   Rev     SDR/DDR     MBits     MBits      MBits     bits   bits   bits
  ------------------------------------------------------------------------------------------------------------------------
  HSB           822866    503539   2     503540   9       4/8     (2) 288 (2)  288 (2)   288 (2)   18*    16*    36*
  PE_1          904058    503541   2     503542   3
  PE_2          904032    503541   2     503542   3
  PE_3          905341    503541   2     503542   3
  PE_4          904316    503541   2     503542   3
  DP_1          915530    504582   6     504583   15
  DP_2          906246    504582   4     504583   15
  DP_3          906230    504582   4     504583   15
```


```
  DP_4          901107   504582  3    504583  15
  IPC           916725   505306  5    505305  16    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base    PWA      PWA     LVM     DBM     ECR
  Name                 Number  Number   Rev     MVec    MBits   MBits
  ---------------------------------------------------------------------
  DBM-DIMM1            507322  505941   1               144
  DBM-DIMM2            507322  505941   1               144
  ECR1-DIMM1           507322  505935   1                       144
  ECR1-DIMM2           507322  505935   1                       144
  ECR2-DIMM1           507322  505935   1                       144
  ECR2-DIMM2           507322  505935   1                       144
  LVM1-DIMM1           505479  505947   1       4
  LVM2-DIMM1           505479  505947   1       4


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
  PSLE2 Fpga     0x1    0x88
  PSS2 Fpga      0x1    0x90
  PSLE3 Fpga     0x1    0x88
  PSS3 Fpga      0x1    0x90
  PSLE4 Fpga     0x1    0x88
  PSS4 Fpga      0x1    0x90
  LVM1 Fpga      0x1    0x4e
  LVM2 Fpga      0x1    0x4f
  ECR1 Fpga      0x1    0xc6
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM_X20 system# XXXXX
HOST computer name: XXXXX
N5VBB: -3.928
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
```


```
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
```


```
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
```


```
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
```


```
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
```


```
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
```


```
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
```


```
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
```

Site2_1_2_VSM_Measure

V5M_Measure	Chassis_1	Slot_2						
V5M_Measure At: 08/23/18 17:23:10 On PEs: 904058 904032 905341 904316 and DPs: 915530 906246 906230 901107								
HostName	XXXXXXX	HSB	822866					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.93	-5.4	-3.93	1.47	-0.15	0.15
Board_1	ADC_2	0	-3.928	-5.4	-3.928	1.473	-0.15	0.15
Board_2	ADC_1	0	-3.93	-5.4	-3.93	1.47	-0.15	0.15
Board_2	ADC_2	0	-3.923	-5.4	-3.923	1.477	-0.15	0.15
Board_3	ADC_1	0	-3.933	-5.4	-3.933	1.467	-0.15	0.15
Board_3	ADC_2	0	-3.916	-5.4	-3.916	1.485	-0.15	0.15
Board_4	ADC_1	0	-3.937	-5.4	-3.937	1.464	-0.15	0.15
Board_4	ADC_2	0	-3.926	-5.4	-3.926	1.475	-0.15	0.15

Site3_1_3

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/23/18 17:23:09
Current Time is: 08/23/18 17:23:12

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXX ***

                                        Site 3 ( Chassis 1, Slot 3 )
  Board         Serial    PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number    Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits    bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           835492    503539  2    503540  9      4/8     (2) 288 (2)  288 (2)   288 (2)  18*   16*   36*
  PE_1          905384    503541  2    503542  3
  PE_2          905394    503541  2    503542  3
  PE_3          905381    503541  2    503542  3
  PE_4          905330    503541  2    503542  3
```

DP_1	902517	504582	4	504583	8	
DP_2	905059	504582	4	504583	8	
DP_3	905116	504582	4	504583	8	
DP_4	905073	504582	4	504583	8	
IPC	916725	505306	5	505305	16	Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	507322	505941	1		144	
DBM-DIMM2	507322	505941	1		144	
ECR1-DIMM1	507322	505935	1			144
ECR1-DIMM2	507322	505935	1			144
ECR2-DIMM1	507322	505935	1			144
ECR2-DIMM2	507322	505935	1			144
LVM1-DIMM1	505479	505947	1	4		
LVM2-DIMM1	505479	505947	1	4		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x9
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f
ECR1 Fpga	0x1	0xc6
ECR2 Fpga	0x1	0xc6

```
Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM_X20 system# XXXXX
HOST computer name: XXXXXX
N5VBB: -3.939
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
```


```
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
```


```
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
```


```
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
```


```
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
```


```
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
```


```
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
```


```
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
         Pass number : 1
         Time for this pass : 00:08:02
         Total time : 00:10:04
Final Bin: pass_bin
Done: 08/23/18 17:31:11
```

Site3_1_3_V5M_Measure

V5M_Measure	Chassis_1	Slot_3						
V5M_Measure At: 08/23/18 17:23:12 On PEs: 905384 905394 905381 905330 and DPs: 902517 905059 905116 905073								
HostName	XXXXX	HSB	835492					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.941	-5.4	-3.941	1.46	-0.15	0.15
Board_1	ADC_2	0	-3.938	-5.4	-3.938	1.462	-0.15	0.15
Board_2	ADC_1	0	-3.941	-5.4	-3.941	1.46	-0.15	0.15
Board_2	ADC_2	0	-3.936	-5.4	-3.936	1.464	-0.15	0.15
Board_3	ADC_1	0	-3.941	-5.4	-3.941	1.459	-0.15	0.15
Board_3	ADC_2	0	-3.931	-5.4	-3.931	1.469	-0.15	0.15
Board_4	ADC_1	0	-3.946	-5.4	-3.946	1.454	-0.15	0.15
Board_4	ADC_2	0	-3.938	-5.4	-3.938	1.462	-0.15	0.15

Site4_1_4

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/23/18 17:23:07
Current Time is: 08/23/18 17:23:11

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXXX ***

                                        Site 4 ( Chassis 1, Slot 4 )
  Board         Serial   PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number   Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits     bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           835546   503539  2    503540  9      2/4     (2) 288 (2)  288 (2)   288 (2)   18*   16*   36*
  PE_1          902179   503541  2    503542  3
  PE_2          905719   503541  2    503542  4
  PE_3          905908   503541  2    503542  4
  PE_4          905708   503541  2    503542  4
  DP_1          910163   504582  6    504583  15
  DP_2          902336   504582  3    504583  15
  DP_3          902337   504582  3    504583  15
```


```
  DP_4          902896   504582  4    504583  15
  IPC           916725   505306  5    505305  16    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base    PWA      PWA     LVM     DBM     ECR
  Name                 Number  Number   Rev     MVec    MBits   MBits
  ---------------------------------------------------------------------
  DBM-DIMM1            505478  505941   1               144
  DBM-DIMM2            505478  505941   1               144
  ECR1-DIMM1           507322  505935   1                       144
  ECR1-DIMM2           507322  505935   1                       144
  ECR2-DIMM1           507322  505935   1                       144
  ECR2-DIMM2           507322  505935   1                       144
  LVM1-DIMM1           505478  505946   1       2
  LVM2-DIMM1           505478  505946   1       2


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
  PSLE2 Fpga     0x1    0x88
  PSS2 Fpga      0x1    0x90
  PSLE3 Fpga     0x1    0x88
  PSS3 Fpga      0x1    0x90
  PSLE4 Fpga     0x1    0x88
  PSS4 Fpga      0x1    0x90
  LVM1 Fpga      0x1    0x4e
  LVM2 Fpga      0x1    0x4f
  ECR1 Fpga      0x1    0xc6
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM_X20 system# XXXXX
HOST computer name: XXXXXX
N5VBB: -3.943
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
```


```
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
```


```
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
```


```
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
```


```
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
```


```
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
```


```
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
```


```
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:03
        Total time : 00:09:58
Final Bin: pass_bin
Done: 08/23/18 17:31:10
```

Site4_1_4_V5M_Measure

V5M_Measure	Chassis_1	Slot_4						
V5M_Measure At: 08/23/18 17:23:11 On PEs: 902179 905719 905908 905708 and DPs: 910163 902336 902337 902896								
HostName	XXXXXXX	HSB	835546					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.942	-5.4	-3.942	1.458	-0.15	0.15
Board_1	ADC_2	0	-3.938	-5.4	-3.938	1.462	-0.15	0.15
Board_2	ADC_1	0	-3.948	-5.4	-3.948	1.452	-0.15	0.15
Board_2	ADC_2	0	-3.938	-5.4	-3.938	1.462	-0.15	0.15
Board_3	ADC_1	0	-3.947	-5.4	-3.947	1.453	-0.15	0.15
Board_3	ADC_2	0	-3.938	-5.4	-3.938	1.462	-0.15	0.15
Board_4	ADC_1	0	-3.95	-5.4	-3.95	1.45	-0.15	0.15
Board_4	ADC_2	0	-3.942	-5.4	-3.942	1.458	-0.15	0.15

System 2

HOST


```
The test program is loading.
The test program is loaded.

Site 1 is the first site in Chassis 1
Site 4 is the last site in Chassis 1
  ui_SiteMask.........: 0xf
  ui_LoadedMask.......: 0xf
  ui_LoadedSlotMask..: 0xf
  ui_LoadedHOBSlotMask..: 0x0
HostName: XXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
ui_TestStarted: Cleared 0 test-done signals.
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
ui_TestDone: Sending test-done signal from 0 to 0
ui_TestStarted: Cleared 1 test-done signals.
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
ui_TestDone: Sending test-done signal from 0 to 0
The test program is unloaded
```

Site1_1_1

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
chassis 1 SET DB_DIAGCMD=1 -> success
TestStarted(1)...

Started: 08/15/18 02:35:48
Current Time is: 08/15/18 02:35:52
```

- Site controller details -
Intel(R) Pentium(R) III CPU - S 1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633

- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXXXX ***

Site 1 (Chassis 1, Slot 1)

Board Name	Serial Number	PWB Number	PWB Rev	PWA Number	PWA Rev	LVM SDR/DDR	DBM MBits	ECR1 MBits	ECR2 MBits	X bits	Y bits	D bits
HSB	830536	503539	2	503540	9	2/4	(2) 288 (2)	288 (2)	288 (2)	18*	16*	36*
PE_1	904653	503541	2	503542	3							
PE_2	901357	503541	2	503542	3							
PE_3	904748	503541	2	503542	3							
PE_4	904911	503541	2	503542	3							
DP_1	909397	504582	6	504583	15							
DP_2	915498	504582	6	504583	15							
DP_3	901802	504582	3	504583	15							
DP_4	903314	504582	4	504583	15							
IPC	839454	505306	3	505305	16	Firmware Revision : 3.6.2						

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	507322	505941	1		144	
DBM-DIMM2	507322	505941	1		144	
ECR1-DIMM1	505479	505935	1			144
ECR1-DIMM2	505479	505935	1			144
ECR2-DIMM1	505479	505935	1			144
ECR2-DIMM2	505479	505935	1			144
LVM1-DIMM1	505478	505946	1	2		
LVM2-DIMM1	505478	505946	1	2		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x9
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f
ECR1 Fpga	0x1	0xc6
ECR2 Fpga	0x1	0xc6

Nextest software release: C:\nextest\h3.9.5A\Bin\Ui.exe


```
Running on UnKnown system# -858993460
HOST computer name: XXXXXXX
N5VBB: -3.928
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
```


```
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
```


```
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
```


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 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
```


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Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
```


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  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
```


```
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:16
        Total time : 00:09:07
Final Bin: pass_bin
Done: 08/15/18 02:44:04
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

TestStarted(2)...

Started: 08/15/18 02:45:25
```


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Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
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  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
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Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
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Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
```


```
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
```


```
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
```


```
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 2
        Time for this pass : 00:07:47
        Total time : 00:18:15
Final Bin: pass_bin
Done: 08/15/18 02:53:12
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

chassis 1 SET DB_DIAGCMD=0 -> success

The test program is unloaded
```

Site1_1_1_V5M_Measure

V5M_Measure	Chassis_1	Slot_1						
V5M_Measure At: 08/15/18 02:35:52 On PEs: 904653 901357 904748 904911 and DPs: 909397 915498 901802 903314								
HostName	XXXXX	HSB	830536					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.935	-5.4	-3.935	1.465	-0.15	0.15
Board_1	ADC_2	0	-3.93	-5.4	-3.93	1.471	-0.15	0.15
Board_2	ADC_1	0	-3.927	-5.4	-3.927	1.473	-0.15	0.15
Board_2	ADC_2	0	-3.917	-5.4	-3.917	1.483	-0.15	0.15
Board_3	ADC_1	0	-3.932	-5.4	-3.932	1.469	-0.15	0.15
Board_3	ADC_2	0	-3.92	-5.4	-3.92	1.481	-0.15	0.15
Board_4	ADC_1	0	-3.939	-5.4	-3.939	1.461	-0.15	0.15
Board_4	ADC_2	0	-3.926	-5.4	-3.926	1.474	-0.15	0.15

Site2_1_2

```
HSB1 SERIAL# XXXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 02:34:06
Current Time is: 08/15/18 02:34:10

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
```

2600.xpsp2.030422-1633

- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXXXXX ***

						Site 2 (Chassis 1, Slot 2)					
Board Name	Serial Number	PWB Number	PWB Rev	PWA Number	PWA Rev	LVM SDR/DDR	DBM MBits	ECR1 MBits	ECR2 MBits	X bits	Y bits	D bits
HSB	822629	503539	2	503540	9	4/8	(2) 288 (2)	288 (2)	288 (2)	18*	16*	36*
PE_1	904658	503541	2	503542	3							
PE_2	901619	503541	2	503542	3							
PE_3	904345	503541	2	503542	3							
PE_4	904314	503541	2	503542	3							
DP_1	908063	504582	5	504583	15							
DP_2	918787	504582	6	504583	15							
DP_3	918587	504582	6	504583	15							
DP_4	914090	504582	6	504583	15							
IPC	839454	505306	3	505305	16	Firmware Revision : 3.6.2						

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	505480	505941	1		144	
DBM-DIMM2	505480	505941	1		144	
ECR1-DIMM1	505479	505935	1			144
ECR1-DIMM2	505479	505935	1			144
ECR2-DIMM1	505479	505935	1			144
ECR2-DIMM2	505479	505935	1			144
LVM1-DIMM1	505478	505947	1	4		
LVM2-DIMM1	505478	505947	1	4		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x9
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f
ECR1 Fpga	0x1	0xc6
ECR2 Fpga	0x1	0xc6

Nextest software release: C:\nextest\h3.9.5A\Bin\Ui.exe
Running on UnKnown system# -858993460
HOST computer name: XXXXXX
N5VBB: -3.930
Testing APG read,write registers via cpu [apg_rw_regs_tb]


```
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
```


```
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
```


```
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
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 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
```


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    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
```


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  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
```


```
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:16
        Total time : 00:08:59
Final Bin: pass_bin
Done: 08/15/18 02:42:22
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

TestStarted(2)...

Started: 08/15/18 02:43:43
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
```


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  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
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  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
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Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
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 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
```


```
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
```


```
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
```


```
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 2
        Time for this pass : 00:07:47
        Total time : 00:18:07
Final Bin: pass_bin
Done: 08/15/18 02:51:30
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site2_1_1_V5M_Measure

V5M_Measure	Chassis_1	Slot_2						
V5M_Measure At: 08/15/18 02:34:10 On PEs: 904658 901619 904345 904314 and DPs: 908063 918787 918587 914090								
HostName	XXXXXXXX	HSB	822629					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.933	-5.4	-3.933	1.468	-0.15	0.15
Board_1	ADC_2	0	-3.927	-5.4	-3.927	1.473	-0.15	0.15
Board_2	ADC_1	0	-3.924	-5.4	-3.924	1.477	-0.15	0.15
Board_2	ADC_2	0	-3.918	-5.4	-3.918	1.482	-0.15	0.15
Board_3	ADC_1	0	-3.938	-5.4	-3.938	1.463	-0.15	0.15
Board_3	ADC_2	0	-3.928	-5.4	-3.928	1.473	-0.15	0.15
Board_4	ADC_1	0	-3.944	-5.4	-3.944	1.457	-0.15	0.15
Board_4	ADC_2	0	-3.929	-5.4	-3.929	1.471	-0.15	0.15

Site3_1_3

```
HSB1 SERIAL# XXXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 02:34:52
Current Time is: 08/15/18 02:34:55

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: XXXXXXX ***

                                          Site 3 ( Chassis 1, Slot 3 )
  Board         Serial    PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number    Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits     bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           835434    503539  2    503540  9      4/8     (2) 288 (2)  288 (2)   288 (2)   18*   16*   36*
  PE_1          905545    503541  2    503542  3
  PE_2          904143    503541  2    503542  3
  PE_3          905574    503541  2    503542  3
  PE_4          904917    503541  2    503542  3
```


```
  DP_1          902476   504582  4    504583  15
  DP_2          907876   504582  5    504583  15
  DP_3          910550   504582  6    504583  15
  DP_4          901849   504582  3    504583  15
  IPC           839454   505306  3    505305  16    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base    PWA      PWA     LVM     DBM     ECR
  Name                 Number  Number   Rev     MVec    MBits   MBits
  ---------------------------------------------------------------------
  DBM-DIMM1            505479  505941   1               144
  DBM-DIMM2            505479  505941   1               144
  ECR1-DIMM1           507322  505935   1                       144
  ECR1-DIMM2           507322  505935   1                       144
  ECR2-DIMM1           507322  505935   1                       144
  ECR2-DIMM2           507322  505935   1                       144
  LVM1-DIMM1           505479  505947   1       4
  LVM2-DIMM1           505479  505947   1       4


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
  PSLE2 Fpga     0x1    0x88
  PSS2 Fpga      0x1    0x90
  PSLE3 Fpga     0x1    0x88
  PSS3 Fpga      0x1    0x90
  PSLE4 Fpga     0x1    0x88
  PSS4 Fpga      0x1    0x90
  LVM1 Fpga      0x1    0x4e
  LVM2 Fpga      0x1    0x4f
  ECR1 Fpga      0x1    0xc6
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on UnKnown system# -858993460
HOST computer name: XXXXXXX
N5VBB: -3.827
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
```


```
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
```


```
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
```


```
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
```


```
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
```


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  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
```


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 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
```


```
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:15
        Total time : 00:08:51
Final Bin: pass_bin
Done: 08/15/18 02:43:07
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

TestStarted(2)...

Started: 08/15/18 02:44:28
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
```


```
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
```


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      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
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 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
```


```
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
```


```
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
```


```
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
```


```
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 2
        Time for this pass : 00:07:48
        Total time : 00:18:00
Final Bin: pass_bin
Done: 08/15/18 02:52:16
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site3_1_3_V5M_Measure

V5M_Measure	Chassis_1	Slot_3						
V5M_Measure At: 08/15/18 02:34:56 On PEs: 905545 904143 905574 904917 and DPs: 902476 907876 910550 901849								
HostName	XXXXXX	HSB	835434					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.827	-5.4	-3.827	1.574	-0.15	0.15
Board_1	ADC_2	0	-3.829	-5.4	-3.829	1.572	-0.15	0.15
Board_2	ADC_1	0	-3.827	-5.4	-3.827	1.573	-0.15	0.15
Board_2	ADC_2	0	-3.821	-5.4	-3.821	1.58	-0.15	0.15
Board_3	ADC_1	0	-3.829	-5.4	-3.829	1.571	-0.15	0.15
Board_3	ADC_2	0	-3.824	-5.4	-3.824	1.577	-0.15	0.15
Board_4	ADC_1	0	-3.833	-5.4	-3.833	1.567	-0.15	0.15
Board_4	ADC_2	0	-3.825	-5.4	-3.825	1.575	-0.15	0.15

Site4_1_4

```
HSB1 SERIAL# XXXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 02:36:16
Current Time is: 08/15/18 02:36:20

- Site controller details -
Intel(R) Pentium(R) III CPU family      1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -

                                                Site 4 ( Chassis 1, Slot 4 )
  Board         Serial    PWB      PWB  PWA      PWA       LVM        DBM       ECR1       ECR2       X      Y      D
  Name          Number    Number   Rev  Number   Rev     SDR/DDR      MBits     MBits      MBits     bits   bits   bits
  ------------------------------------------------------------------------------------------------------------------------
  HSB           822790    503539   2    503540   9       16/32    (2) 288 (2)  288 (2)    288 (2)   18*    16*    36*
  PE_1          904166    503541   2    503542   3
  PE_2          904158    503541   2    503542   3
  PE_3          904173    503541   2    503542   3
  PE_4          904165    503541   2    503542   3
```


```
  DP_1          902574   504582  4    504583  15
  DP_2          902942   504582  4    504583  15
  DP_3          902927   504582  4    504583  15
  DP_4          914230   504582  6    504583  15
  IPC           839454   505306  3    505305  16    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base    PWA      PWA     LVM     DBM     ECR
  Name                 Number  Number   Rev     MVec    MBits   MBits
  ---------------------------------------------------------------------
  DBM-DIMM1            507322  505941   1               144
  DBM-DIMM2            507322  505941   1               144
  ECR1-DIMM1           505478  505935   1                       144
  ECR1-DIMM2           505478  505935   1                       144
  ECR2-DIMM1           505478  505935   1                       144
  ECR2-DIMM2           505478  505935   1                       144
  LVM1-DIMM1           505479  505949   1       16
  LVM2-DIMM1           505479  505949   1       16


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
  PSLE2 Fpga     0x1    0x88
  PSS2 Fpga      0x1    0x90
  PSLE3 Fpga     0x1    0x88
  PSS3 Fpga      0x1    0x90
  PSLE4 Fpga     0x1    0x88
  PSS4 Fpga      0x1    0x90
  LVM1 Fpga      0x1    0x4e
  LVM2 Fpga      0x1    0x4f
  ECR1 Fpga      0x1    0xc6
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on UnKnown system# -858993460
HOST computer name: XXXXXXX
N5VBB: -3.769
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
```


```
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
```


```
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
```


```
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
```


```
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
```


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  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
```


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 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
```


```
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:15
        Total time : 00:08:43
Final Bin: pass_bin
Done: 08/15/18 02:44:31
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

TestStarted(2)...

Started: 08/15/18 02:45:53
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
```


```
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                 Setting up background data
                 Test and write complement with ascending address
                 Test and write complement with descending address
                 Setting up background data
                 Test and write complement with ascending address
                 Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                 Setting up background data
                 Test and write complement with ascending address
                 Test and write complement with descending address
                 Setting up background data
                 Test and write complement with ascending address
                 Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
```


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    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
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 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
```


```
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
```


```
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
```


```
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
```


```
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 2
        Time for this pass : 00:07:47
        Total time : 00:17:52
Final Bin: pass_bin
Done: 08/15/18 02:53:40
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site4_1_4_V5M_Measure

V5M_Measure	Chassis_1	Slot_4						
V5M_Measure At: 08/15/18 02:36:20 On PEs: 904166 904158 904173 904165 and DPs: 902574 902942 902927 914230								
HostName	XXXXXX	HSB	822790					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.771	-5.4	-3.771	1.629	-0.15	0.15
Board_1	ADC_2	0	-3.768	-5.4	-3.768	1.633	-0.15	0.15
Board_2	ADC_1	0	-3.775	-5.4	-3.775	1.626	-0.15	0.15
Board_2	ADC_2	0	-3.767	-5.4	-3.767	1.633	-0.15	0.15
Board_3	ADC_1	0	-3.767	-5.4	-3.767	1.634	-0.15	0.15
Board_3	ADC_2	0	-3.756	-5.4	-3.756	1.645	-0.15	0.15
Board_4	ADC_1	0	-3.78	-5.4	-3.78	1.62	-0.15	0.15
Board_4	ADC_2	0	-3.77	-5.4	-3.77	1.63	-0.15	0.15

System 3

HOST

```
The test program is loading.
The test program is loaded.

Site 1 is the first site in Chassis 1
Site 4 is the last site in Chassis 1
  ui_SiteMask.........: 0xf
  ui_LoadedMask......: 0xf
  ui_LoadedSlotMask..: 0xf
  ui_LoadedHOBSlotMask..: 0x0
HostName: XXXXXX
Nextest software release: C:\nextest\h3.9.5A
ui_TestStarted: Cleared 0 test-done signals.
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
ui_TestDone: Sending test-done signal from 0 to 0
The test program is unloaded
```

Site1_1_1

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXX
Nextest software release: C:\nextest\h3.9.5A
chassis 1 SET DB_DIAGCMD=1 -> success
TestStarted(1)...

Started: 08/15/18 03:17:30
Current Time is: 08/15/18 03:17:34

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

                                                Site 1  ( Chassis 1, Slot 1 )
  Board         Serial   PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number   Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits     bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           830477   503539  2    503540  9      16/32   (2) 288 (2)  288 (2)   288 (2)   18*   16*   36*
  PE_1          901535   503541  2    503542  3
  PE_2          905923   503541  2    503542  4
  PE_3          902023   503541  2    503542  4
  PE_4          904551   503541  2    503542  3
  DP_1          914039   504582  6    504583  15
  DP_2          906082   504582  4    504583  15
  DP_3          901111   504582  3    504583  15
  DP_4          903441   504582  4    504583  15
  IPC           117003   505306  5    505305  20    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base     PWA      PWA     LVM     DBM     ECR
  Name                 Number   Number   Rev     MVec    MBits   MBits
  ------------------------------------------------------------------
  DBM-DIMM1            505479   505941   1               144
  DBM-DIMM2            505479   505941   1               144
  ECR1-DIMM1           505479   505935   1                       144
  ECR1-DIMM2           505479   505935   1                       144
  ECR2-DIMM1           505479   505935   1                       144
  ECR2-DIMM2           505479   505935   1                       144
  LVM1-DIMM1           505480   505949   1       16
  LVM2-DIMM1           505480   505949   1       16


- Revision Codes for FPGAs -
  FPGA          SW     HW
  Name          Rev    Rev
```


```
  -------------------------
  CPUI Fpga       0x1    0x9
  TG1 Fpga        0x1    0x18
  TG2 Fpga        0x1    0x18
  TG3 Fpga        0x1    0x18
  TG4 Fpga        0x1    0x18
  TG5 Fpga        0x1    0x18
  TG6 Fpga        0x1    0x18
  TG7 Fpga        0x1    0x18
  TG8 Fpga        0x1    0x18
  APG1 Fpga       0x1    0xf3
  APG2 Fpga       0x1    0xb0
  DBM1 Fpga       0x1    0xbf
  PSLE1 Fpga      0x1    0x88
  PSS1 Fpga       0x1    0x90
  PSLE2 Fpga      0x1    0x88
  PSS2 Fpga       0x1    0x90
  PSLE3 Fpga      0x1    0x88
  PSS3 Fpga       0x1    0x90
  PSLE4 Fpga      0x1    0x88
  PSS4 Fpga       0x1    0x90
  LVM1 Fpga       0x1    0x4e
  LVM2 Fpga       0x1    0x4f
  ECR1 Fpga       0x1    0xc6
  ECR2 Fpga       0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXX
HOST computer name: XXXXX
N5VBB: -3.514
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
         Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
```


```
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
```


```
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
```


```
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
```


```
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
```


```
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
```


```
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
```


```
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:08
        Total time : 00:08:48
Final Bin: pass_bin
Done: 08/15/18 03:25:38
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

chassis 1 SET DB_DIAGCMD=0 -> success

The test program is unloaded
```

Site1_1_1_V5M_Measure

V5M_Measure	Chassis_1	Slot_1						
V5M_Measure At: 08/15/18 03:17:34 On PEs: 901535 905923 902023 904551 and DPs: 914039 906082 901111 903441								
HostName	XXXXXX	HSB	830477					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.514	-5.4	-3.514	1.886	-0.15	0.15
Board_1	ADC_2	0	-3.508	-5.4	-3.508	1.892	-0.15	0.15
Board_2	ADC_1	0	-3.519	-5.4	-3.519	1.882	-0.15	0.15
Board_2	ADC_2	0	-3.514	-5.4	-3.514	1.887	-0.15	0.15
Board_3	ADC_1	0	-3.517	-5.4	-3.517	1.883	-0.15	0.15
Board_3	ADC_2	0	-3.506	-5.4	-3.506	1.894	-0.15	0.15
Board_4	ADC_1	0	-3.521	-5.4	-3.521	1.879	-0.15	0.15
Board_4	ADC_2	0	-3.514	-5.4	-3.514	1.886	-0.15	0.15

Site2_1_2

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
```


```
The test program is loaded

HostName: XXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 03:18:26
Current Time is: 08/15/18 03:18:30

- Site controller details -
Intel(R) Pentium(R) III CPU family      1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -

                                                Site 2  ( Chassis 1, Slot 2 )
  Board         Serial   PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number   Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits    bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           835414   503539  2    503540  9      2/4     (2) 288 (2)  288 (2)   288 (2)  18*   16*   36*
  PE_1          904063   503541  2    503542  3
  PE_2          904816   503541  2    503542  3
  PE_3          904933   503541  2    503542  3
  PE_4          902190   503541  2    503542  3
  DP_1          912101   504582  6    504583  15
  DP_2          906196   504582  4    504583  15
  DP_3          901177   504582  3    504583  15
  DP_4          918715   504582  6    504583  15
  IPC           117003   505306  5    505305  20    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base     PWA      PWA     LVM     DBM     ECR
  Name                 Number   Number   Rev     MVec    MBits   MBits
  ------------------------------------------------------------------
  DBM-DIMM1            505479   505941   1               144
  DBM-DIMM2            505479   505941   1               144
  ECR1-DIMM1           507322   505935   1                       144
  ECR1-DIMM2           507322   505935   1                       144
  ECR2-DIMM1           505479   505935   1                       144
  ECR2-DIMM2           505479   505935   1                       144
  LVM1-DIMM1           505478   505946   1       2
  LVM2-DIMM1           505478   505946   1       2


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
  PSLE2 Fpga     0x1    0x88
  PSS2 Fpga      0x1    0x90
  PSLE3 Fpga     0x1    0x88
  PSS3 Fpga      0x1    0x90
  PSLE4 Fpga     0x1    0x88
```


```
  PSS4 Fpga       0x1    0x90
  LVM1 Fpga       0x1    0x4e
  LVM2 Fpga       0x1    0x4f
  ECR1 Fpga       0x1    0xc6
  ECR2 Fpga       0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXX
HOST computer name: XXXXX
N5VBB: -3.681
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
         Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
```


```
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
```


```
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
```


```
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
```


```
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
```


```
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
```


```
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:08
        Total time : 00:08:41
```


```
Final Bin: pass_bin
Done: 08/15/18 03:26:34
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site2_1_2_V5M_Measure

V5M_Measure	Chassis_1	Slot_2						
V5M_Measure At: 08/15/18 03:18:30 On PEs: 904063 904816 904933 902190 and DPs: 912101 906196 901177 918715								
HostName	XXXXXX	HSB	835414					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.683	-5.4	-3.683	1.718	-0.15	0.15
Board_1	ADC_2	0	-3.679	-5.4	-3.679	1.722	-0.15	0.15
Board_2	ADC_1	0	-3.684	-5.4	-3.684	1.716	-0.15	0.15
Board_2	ADC_2	0	-3.676	-5.4	-3.676	1.724	-0.15	0.15
Board_3	ADC_1	0	-3.682	-5.4	-3.682	1.718	-0.15	0.15
Board_3	ADC_2	0	-3.678	-5.4	-3.678	1.722	-0.15	0.15
Board_4	ADC_1	0	-3.687	-5.4	-3.687	1.713	-0.15	0.15
Board_4	ADC_2	0	-3.68	-5.4	-3.68	1.721	-0.15	0.15

Site3_1_3

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 03:17:33
Current Time is: 08/15/18 03:17:36
```

- Site controller details -
Intel(R) Pentium(R) III CPU - S 1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633

- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

Site 3 (Chassis 1, Slot 3)

Board Name	Serial Number	PWB Number	PWB Rev	PWA Number	PWA Rev	LVM SDR/DDR	DBM MBits	ECR1 MBits	ECR2 MBits	X bits	Y bits	D bits
HSB	830557	503539	2	503540	10	4/8	(2) 288 (2)	288 (2)	288 (2)	18*	16*	36*
PE_1	901657	503541	2	503542	3							
PE_2	904067	503541	2	503542	3							
PE_3	904664	503541	2	503542	4							
PE_4	904803	503541	2	503542	3							
DP_1	910421	504582	6	504583	15							
DP_2	903182	504582	4	504583	7							
DP_3	903174	504582	4	504583	7							
DP_4	915308	504582	6	504583	15							
IPC	117003	505306	5	505305	20	Firmware Revision : 3.6.2						

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	505479	505941	1		144	
DBM-DIMM2	505479	505941	1		144	
ECR1-DIMM1	507322	505935	1			144
ECR1-DIMM2	507322	505935	1			144
ECR2-DIMM1	507322	505935	1			144
ECR2-DIMM2	507322	505935	1			144
LVM1-DIMM1	505478	505947	1	4		
LVM2-DIMM1	505478	505947	1	4		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0xa
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f
ECR1 Fpga	0x1	0xc6
ECR2 Fpga	0x1	0xc6

Nextest software release: C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXX


```
HOST computer name: XXXXXX
N5VBB: -3.679
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
         Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
```


```
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
```


```
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
```


```
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
```


```
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
```


```
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
```


```
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:08
        Total time : 00:08:34
Final Bin: pass_bin
Done: 08/15/18 03:25:41
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site3_1_3_V5M_Measure

V5M_Measure	Chassis_1	Slot_3						
V5M_Measure At: 08/15/18 03:17:36 On PEs: 901657 904067 904664 904803 and DPs: 910421 903182 903174 915308								
HostName	XXXXX	HSB	830557					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.677	-5.4	-3.677	1.723	-0.15	0.15
Board_1	ADC_2	0	-3.671	-5.4	-3.671	1.73	-0.15	0.15
Board_2	ADC_1	0	-3.684	-5.4	-3.684	1.717	-0.15	0.15
Board_2	ADC_2	0	-3.675	-5.4	-3.675	1.726	-0.15	0.15
Board_3	ADC_1	0	-3.68	-5.4	-3.68	1.72	-0.15	0.15
Board_3	ADC_2	0	-3.676	-5.4	-3.676	1.725	-0.15	0.15
Board_4	ADC_1	0	-3.688	-5.4	-3.688	1.712	-0.15	0.15
Board_4	ADC_2	0	-3.68	-5.4	-3.68	1.72	-0.15	0.15

Site4_1_4

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 03:18:32
Current Time is: 08/15/18 03:18:36

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

                                        Site 4 ( Chassis 1, Slot 4 )
  Board         Serial    PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2       X     Y     D
  Name          Number    Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits     bits  bits  bits
```

HSB	822878	503539	2	503540	9	4/8	(2) 288 (2)	288 (2)	288 (2)	18*	16*	36*
PE_1	904242	503541	2	503542	3							
PE_2	904494	503541	2	503542	3							
PE_3	840712	503541	2	503542	3							
PE_4	904276	503541	2	503542	3							
DP_1	918719	504582	6	504583	15							
DP_2	903178	504582	4	504583	15							
DP_3	903463	504582	4	504583	15							
DP_4	903432	504582	4	504583	15							
IPC	117003	505306	5	505305	20	Firmware Revision : 3.6.2						

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	505479	505941	1		144	
DBM-DIMM2	505479	505941	1		144	
ECR1-DIMM1	505479	505935	1			144
ECR1-DIMM2	505479	505935	1			144
ECR2-DIMM1	505479	505935	1			144
ECR2-DIMM2	505479	505935	1			144
LVM1-DIMM1	505479	505947	1	4		
LVM2-DIMM1	505479	505947	1	4		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x9
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f
ECR1 Fpga	0x1	0xc6
ECR2 Fpga	0x1	0xc6

```
Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXXX
HOST computer name: XXXXXXX
N5VBB: -3.666
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
```


```
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
         Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
```


```
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
```


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 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
```


```
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
```


```
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
```


```
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
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   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:08
        Total time : 00:08:26
Final Bin: pass_bin
Done: 08/15/18 03:26:40
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site4_1_4_V5M_Measure

V5M_Measure	Chassis_1	Slot_4						
V5M_Measure At: 08/15/18 03:18:36 On PEs: 904242 904494 840712 904276 and DPs: 918719 903178 903463 903432								
HostName	XXXXX	HSB	822878					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.663	-5.4	-3.663	1.738	-0.15	0.15
Board_1	ADC_2	0	-3.658	-5.4	-3.658	1.742	-0.15	0.15
Board_2	ADC_1	0	-3.678	-5.4	-3.678	1.723	-0.15	0.15
Board_2	ADC_2	0	-3.667	-5.4	-3.667	1.733	-0.15	0.15
Board_3	ADC_1	0	-3.668	-5.4	-3.668	1.733	-0.15	0.15
Board_3	ADC_2	0	-3.662	-5.4	-3.662	1.739	-0.15	0.15
Board_4	ADC_1	0	-3.67	-5.4	-3.67	1.73	-0.15	0.15
Board_4	ADC_2	0	-3.662	-5.4	-3.662	1.738	-0.15	0.15

System 4

HOST

```
The test program is loading.
The test program is loaded.

Site 1 is the first site in Chassis 1
Site 4 is the last site in Chassis 1
  ui_SiteMask.........: 0xf
  ui_LoadedMask......: 0xf
  ui_LoadedSlotMask..: 0xf
  ui_LoadedHOBSlotMask..: 0x0
HostName: XXXXX
Nextest software release: C:\nextest\h3.9.5A
ui_TestStarted: Cleared 0 test-done signals.
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
ui_TestDone: Sending test-done signal from 0 to 0
The test program is unloaded
```

Site1_1_1

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXX
Nextest software release: C:\nextest\h3.9.5A
chassis 1 SET DB_DIAGCMD=1 -> success
TestStarted(1)...

Started: 08/15/18 09:15:10
Current Time is: 08/15/18 09:15:14

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

                                          Site 1 ( Chassis 1, Slot 1 )
  Board         Serial   PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number   Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits    bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           822590   503539  2    503540  9      4/8     (2) 288 (2)  288 (2)   288 (2)  18*   16*   36*
  PE_1          904616   503541  2    503542  3
  PE_2          904221   503541  2    503542  3
  PE_3          904213   503541  2    503542  3
  PE_4          904233   503541  2    503542  3
  DP_1          903249   504582  4    504583  7
  DP_2          912146   504582  6    504583  15
  DP_3          907969   504582  5    504583  15
  DP_4          903266   504582  4    504583  7
  IPC           945121   505306  5    505305  16    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base     PWA      PWA     LVM     DBM     ECR
  Name                 Number   Number   Rev     MVec    MBits   MBits
  ------------------------------------------------------------------
  DBM-DIMM1            507322   505941   1               144
  DBM-DIMM2            507322   505941   1               144
  ECR1-DIMM1           507322   505935   1                       144
  ECR1-DIMM2           507322   505935   1                       144
  ECR2-DIMM1           507322   505935   1                       144
  ECR2-DIMM2           507322   505935   1                       144
  LVM1-DIMM1           505479   505947   1       4
  LVM2-DIMM1           505479   505947   1       4
```


```
- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
  PSLE2 Fpga     0x1    0x88
  PSS2 Fpga      0x1    0x90
  PSLE3 Fpga     0x1    0x88
  PSS3 Fpga      0x1    0x90
  PSLE4 Fpga     0x1    0x88
  PSS4 Fpga      0x1    0x90
  LVM1 Fpga      0x1    0x4e
  LVM2 Fpga      0x1    0x4f
  ECR1 Fpga      0x1    0xc6
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXXX
HOST computer name: XXXXXX
N5VBB: -3.684
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
         Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
```


```
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
```


```
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
```


```
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
```


```
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
```


```
        PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
```


```
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
```


```
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:33
        Total time : 00:09:06
Final Bin: pass_bin
Done: 08/15/18 09:23:43
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

chassis 1 SET DB_DIAGCMD=0 -> success

The test program is unloaded
```

Site1_1_1_V5M_Measure

V5M_Measure	Chassis_1	Slot_1						
V5M_Measure At: 08/15/18 09:15:14 On PEs: 904616 904221 904213 904233 and DPs: 903249 912146 907969 903266								
HostName	XXXXX	HSB	822590					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.69	-5.4	-3.69	1.71	-0.15	0.15
Board_1	ADC_2	0	-3.688	-5.4	-3.688	1.712	-0.15	0.15
Board_2	ADC_1	0	-3.688	-5.4	-3.688	1.713	-0.15	0.15
Board_2	ADC_2	0	-3.684	-5.4	-3.684	1.716	-0.15	0.15
Board_3	ADC_1	0	-3.68	-5.4	-3.68	1.72	-0.15	0.15
Board_3	ADC_2	0	-3.671	-5.4	-3.671	1.729	-0.15	0.15
Board_4	ADC_1	0	-3.691	-5.4	-3.691	1.709	-0.15	0.15
Board_4	ADC_2	0	-3.684	-5.4	-3.684	1.717	-0.15	0.15

Site2_1_2

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
```


```
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 09:15:10
Current Time is: 08/15/18 09:15:14

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

                                          Site 2 ( Chassis 1, Slot 2 )
  Board         Serial   PWB     PWB  PWA     PWA      LVM       DBM      ECR1      ECR2      X     Y     D
  Name          Number   Number  Rev  Number  Rev    SDR/DDR     MBits    MBits     MBits    bits  bits  bits
  ------------------------------------------------------------------------------------------------------------
  HSB           822808   503539  2    503540  9      4/8     (2) 288 (2)  288 (2)   288 (2)  18*   16*   36*
  PE_1          901336   503541  2    503542  3
  PE_2          905938   503541  2    503542  4
  PE_3          904697   503541  2    503542  4
  PE_4          904926   503541  2    503542  3
  DP_1          910253   504582  6    504583  15
  DP_2          902371   504582  3    504583  15
  DP_3          912015   504582  6    504583  15
  DP_4          902353   504582  3    504583  15
  IPC           945121   505306  5    505305  16    Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module               Base     PWA      PWA     LVM     DBM     ECR
  Name                 Number   Number   Rev     MVec    MBits   MBits
  ------------------------------------------------------------------
  DBM-DIMM1            505478   505941   1               144
  DBM-DIMM2            507322   505941   1               144
  ECR1-DIMM1           505479   505935   1                       144
  ECR1-DIMM2           505479   505935   1                       144
  ECR2-DIMM1           505479   505935   1                       144
  ECR2-DIMM2           505479   505935   1                       144
  LVM1-DIMM1           505479   505947   1       4
  LVM2-DIMM1           505479   505947   1       4


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
```


```
  TG5 Fpga        0x1    0x18
  TG6 Fpga        0x1    0x18
  TG7 Fpga        0x1    0x18
  TG8 Fpga        0x1    0x18
  APG1 Fpga       0x1    0xf3
  APG2 Fpga       0x1    0xb0
  DBM1 Fpga       0x1    0xbf
  PSLE1 Fpga      0x1    0x88
  PSS1 Fpga       0x1    0x90
  PSLE2 Fpga      0x1    0x88
  PSS2 Fpga       0x1    0x90
  PSLE3 Fpga      0x1    0x88
  PSS3 Fpga       0x1    0x90
  PSLE4 Fpga      0x1    0x88
  PSS4 Fpga       0x1    0x90
  LVM1 Fpga       0x1    0x4e
  LVM2 Fpga       0x1    0x4f
  ECR1 Fpga       0x1    0xc6
  ECR2 Fpga       0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXXX
HOST computer name: XXXXXX
N5VBB: -3.682
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
```


```
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
```


```
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
```


```
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
```


```
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
```


```
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
```


```
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
```


```
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:33
        Total time : 00:09:00
Final Bin: pass_bin
Done: 08/15/18 09:23:43
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site2_1_2_V5M_Measure

V5M_Measure	Chassis_1	Slot_2						
V5M_Measure At: 08/15/18 09:15:14 On PEs: 901336 905938 904697 904926 and DPs: 910253 902371 912015 902353								
HostName	XXXXXXX	HSB	822808					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.683	-5.4	-3.683	1.717	-0.15	0.15
Board_1	ADC_2	0	-3.678	-5.4	-3.678	1.722	-0.15	0.15
Board_2	ADC_1	0	-3.683	-5.4	-3.683	1.718	-0.15	0.15
Board_2	ADC_2	0	-3.68	-5.4	-3.68	1.721	-0.15	0.15
Board_3	ADC_1	0	-3.688	-5.4	-3.688	1.713	-0.15	0.15
Board_3	ADC_2	0	-3.676	-5.4	-3.676	1.724	-0.15	0.15
Board_4	ADC_1	0	-3.689	-5.4	-3.689	1.711	-0.15	0.15
Board_4	ADC_2	0	-3.678	-5.4	-3.678	1.722	-0.15	0.15

Site3_1_3

```
HSB1 SERIAL# XXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
```


```
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...

Started: 08/15/18 09:15:10
Current Time is: 08/15/18 09:15:14

- Site controller details -
Intel(R) Pentium(R) III CPU - S         1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633


- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

                                                Site 3 ( Chassis 1, Slot 3 )
  Board          Serial    PWB      PWB   PWA      PWA       LVM        DBM       ECR1       ECR2       X      Y      D
  Name           Number    Number   Rev   Number   Rev     SDR/DDR      MBits     MBits      MBits      bits   bits   bits
  ---------------------------------------------------------------------------------------------------------------------
  HSB            835536    503539   2     503540   9       16/32   (2)  288 (2)   288 (2)    288 (2)    18*    16*    36*
  PE_1           905331    503541   2     503542   3
  PE_2           901498    503541   2     503542   3
  PE_3           901353    503541   2     503542   3
  PE_4           905945    503541   2     503542   4
  DP_1           903232    504582   4     504583   15
  DP_2           902857    504582   4     504583   15
  DP_3           918641    504582   6     504583   15
  DP_4           910282    504582   6     504583   15
  IPC            945121    505306   5     505305   16     Firmware Revision : 3.6.2

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.


- Revision Codes for Memory Modules -
  Module                 Base     PWA      PWA      LVM      DBM      ECR
  Name                   Number   Number   Rev      MVec     MBits    MBits
  ---------------------------------------------------------------------
  DBM-DIMM1              505478   505941   1                 144
  DBM-DIMM2              507322   505941   1                 144
  ECR1-DIMM1             507322   505935   1                          144
  ECR1-DIMM2             507322   505935   1                          144
  ECR2-DIMM1             507322   505935   1                          144
  ECR2-DIMM2             507322   505935   1                          144
  LVM1-DIMM1             505480   505949   1        16
  LVM2-DIMM1             505480   505949   1        16


- Revision Codes for FPGAs -
  FPGA           SW     HW
  Name           Rev    Rev
  -------------------------
  CPUI Fpga      0x1    0x9
  TG1 Fpga       0x1    0x18
  TG2 Fpga       0x1    0x18
  TG3 Fpga       0x1    0x18
  TG4 Fpga       0x1    0x18
  TG5 Fpga       0x1    0x18
  TG6 Fpga       0x1    0x18
  TG7 Fpga       0x1    0x18
  TG8 Fpga       0x1    0x18
  APG1 Fpga      0x1    0xf3
  APG2 Fpga      0x1    0xb0
  DBM1 Fpga      0x1    0xbf
  PSLE1 Fpga     0x1    0x88
  PSS1 Fpga      0x1    0x90
```


```
  PSLE2 Fpga      0x1    0x88
  PSS2 Fpga       0x1    0x90
  PSLE3 Fpga      0x1    0x88
  PSS3 Fpga       0x1    0x90
  PSLE4 Fpga      0x1    0x88
  PSS4 Fpga       0x1    0x90
  LVM1 Fpga       0x1    0x4e
  LVM2 Fpga       0x1    0x4f
  ECR1 Fpga       0x1    0xc6
  ECR2 Fpga       0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXX
HOST computer name: XXXXX
N5VBB: -3.678
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
        Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
        Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
        Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
                Setting up background data
                Test and write complement with ascending address
                Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
```


```
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
```


```
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
```


```
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
```


```
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
```


```
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
```


```
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
  Testing 4 Sites-per-Controller
```


```
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:33
        Total time : 00:08:52
Final Bin: pass_bin
Done: 08/15/18 09:23:43
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin


The test program is unloaded
```

Site3_1_3_V5M_Measure

V5M_Measure	Chassis_1	Slot_3						
V5M_Measure At: 08/15/18 09:15:14 On PEs: 905331 901498 901353 905945 and DPs: 903232 902857 918641 910282								
HostName	XXXXXX	HSB	835536					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.689	-5.4	-3.689	1.711	-0.15	0.15
Board_1	ADC_2	0	-3.684	-5.4	-3.684	1.716	-0.15	0.15
Board_2	ADC_1	0	-3.678	-5.4	-3.678	1.723	-0.15	0.15
Board_2	ADC_2	0	-3.671	-5.4	-3.671	1.73	-0.15	0.15
Board_3	ADC_1	0	-3.67	-5.4	-3.67	1.73	-0.15	0.15
Board_3	ADC_2	0	-3.665	-5.4	-3.665	1.735	-0.15	0.15
Board_4	ADC_1	0	-3.689	-5.4	-3.689	1.711	-0.15	0.15
Board_4	ADC_2	0	-3.68	-5.4	-3.68	1.721	-0.15	0.15

Site4_1_4

```
HSB1 SERIAL# XXXXXX
Loading VCAL Data on t_hsb1, t_pe32_1
Loading VCAL Data on t_hsb1, t_pe32_2
Loading VCAL Data on t_hsb1, t_pe32_3
Loading VCAL Data on t_hsb1, t_pe32_4
Loading VCAL Data on t_hsb1, t_dps_pmu_1
Loading VCAL Data on t_hsb1, t_dps_pmu_2
Loading VCAL Data on t_hsb1, t_dps_pmu_3
Loading VCAL Data on t_hsb1, t_dps_pmu_4
Loading TCal data from file: Y:\nextest\caldata\tcal_data_XXXXXX.bin
Loading TCal TDR  data from DUT board EEPROM
Creating pattern set => Logic_set
Creating pattern set => PE32_ps_ddr_set
Creating pattern set => PE32_ps_set
Creating pattern set => PE32_tg_set
Creating pattern set => default_set
The test program is loaded

HostName: XXXXXX
Nextest software release: C:\nextest\h3.9.5A
TestStarted(1)...
```

Started: 08/15/18 09:15:10
Current Time is: 08/15/18 09:15:14

- Site controller details -
Intel(R) Pentium(R) III CPU - S 1266MHz, 497MB total physical memory.
Microsoft Windows XP
2600.xpsp2.030422-1633

- Revision Codes for Boards -
*** Summary of board set for SA pn: 505701 ***

Site 4 (Chassis 1, Slot 4)

Board Name	Serial Number	PWB Number	PWB Rev	PWA Number	PWA Rev	LVM SDR/DDR	DBM MBits	ECR1 MBits	ECR2 MBits	X bits	Y bits	D bits
HSB	819631	503539	2	503540	9	2/4	(2) 288 (2)	288 (2)	288 (2)	18*	16*	36*
PE_1	901457	503541	2	503542	3							
PE_2	901384	503541	2	503542	3							
PE_3	901290	503541	2	503542	3							
PE_4	901466	503541	2	503542	3							
DPX20_1	929208	504582	7	508488	1							
DPX20_2	932536	504582	7	508488	1							
DPX20_3	929163	504582	7	508488	1							
DPX20_4	922166	504582	7	508488	1							
IPC	945121	505306	5	505305	16	Firmware Revision : 3.6.2						

* NOTE: The ECR X, Y, D bits represent the maximum allowable configuration.

- Revision Codes for Memory Modules -

Module Name	Base Number	PWA Number	PWA Rev	LVM MVec	DBM MBits	ECR MBits
DBM-DIMM1	507322	505939	1		144	
DBM-DIMM2	505478	505941	1		144	
ECR1-DIMM1	505480	505935	1			144
ECR1-DIMM2	505480	505935	1			144
ECR2-DIMM1	505480	505935	1			144
ECR2-DIMM2	505480	505935	1			144
LVM1-DIMM1	505478	505946	1	2		
LVM2-DIMM1	505458	505946	1	2		

- Revision Codes for FPGAs -

FPGA Name	SW Rev	HW Rev
CPUI Fpga	0x1	0x9
TG1 Fpga	0x1	0x18
TG2 Fpga	0x1	0x18
TG3 Fpga	0x1	0x18
TG4 Fpga	0x1	0x18
TG5 Fpga	0x1	0x18
TG6 Fpga	0x1	0x18
TG7 Fpga	0x1	0x18
TG8 Fpga	0x1	0x18
APG1 Fpga	0x1	0xf3
APG2 Fpga	0x1	0xb0
DBM1 Fpga	0x1	0xbf
PSLE1 Fpga	0x1	0x88
PSS1 Fpga	0x1	0x90
PSLE2 Fpga	0x1	0x88
PSS2 Fpga	0x1	0x90
PSLE3 Fpga	0x1	0x88
PSS3 Fpga	0x1	0x90
PSLE4 Fpga	0x1	0x88
PSS4 Fpga	0x1	0x90
LVM1 Fpga	0x1	0x4e
LVM2 Fpga	0x1	0x4f
ECR1 Fpga	0x1	0xc6


```
  ECR2 Fpga      0x1    0xc6

Nextest software release:  C:\nextest\h3.9.5A\Bin\Ui.exe
Running on MAGNUM system# XXXXXX
HOST computer name: XXXXXX
N5VBB: -3.668
Testing APG read,write registers via cpu [apg_rw_regs_tb]
  Testing Address registers and LBDATA
  Testing MAR and INTA
  Testing JAM, DMAIN, DBASE, YINDEX
  Testing Unique values
Testing APG counter RAM - short march [apg_counter_ram_short_march_tb]
Testing APG reload RAM - short march [apg_reload_ram_short_march_tb]
Testing APG XDTOPO RAM - short march [apg_xdtopo_ram_short_march_tb]
Testing APG YDTOPO RAM - short march [apg_ydtopo_ram_short_march_tb]
Testing APG uRAM - short march [apg_uram_ram_short_march_tb]
Testing APG Cycle Length RAM - short march [apg_cycle_ram_short_march_tb]
Testing APG DAC RAM - short march [apg_dac_ram_short_march_tb]
Testing APG XTOPO RAM - short march [apg_xtopo_ram_short_march_tb]
Testing APG YTOPO RAM - short march [apg_ytopo_ram_short_march_tb]
Testing APG User RAM - short march [apg_user_ram_short_march_tb]
Testing APG vRAM - short march [apg_vram_ram_short_march_tb]
         Testing APG vRAM VMC1 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC1 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
         Testing APG vRAM VMC2 DIMM1 - Bit Independence Test
         Testing APG vRAM VMC2 DIMM1 - Address Independence Test
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
                  Setting up background data
                  Test and write complement with ascending address
                  Test and write complement with descending address
Testing HSB 100Mhz clock frequency [hsb_clk_check_tb]
Testing APG counter functions [apg_counter_tests_tb]
    Pattern start is at 4bc
  Testing Counter loading
  Testing Counter address
  Testing Reload loading
  Testing Reload address
  Testing Reload counters from reload registers
  Testing Counter DECR
  Testing Counter INCR
  Testing Counter DECR2
Testing MAR increments, stack nesting [apg_mar_and_stack_tests_tb]
  Testing MAR increments
  Testing Stack nesting, 1st pass
  Testing Stack nesting, 2nd pass
   Stack nesting, 50nS
   Stack nesting, 20nS
Testing APG counter branching [apg_counter_branching_tb]
    Pattern start is at 5f8
Testing APG timer branching and accuracy [apg_timer_branching_tb]
    Pattern start is at bd
Testing APG interrupt branch logic and addressing [apg_interrupt_branching_tb]
    Pattern start is at 6f6
Testing APG address generators [apg_address_generators_tb]
    Pattern start is at 607
  Testing uDATA loads
  Testing COMP function
  Testing logic functions
  Testing add
  Testing subtract
  Testing decrement and increment
  Testing Y to X carries and borrows
  Testing X to Y carries and borrows
Testing APG data generator [apg_data_generator_tb]
```


```
    Pattern start is at 69
  Testing uDATA loads
  Testing Count up and down with shift left, 18 bit DMAIN register
  Testing Count up and down with shift left, 18 bit DBASE register
  Testing Shift right, 18 bit DMAIN register
  Testing Shift right, 18 bit DBASE register
  Testing Rotate left, 18 bit DMAIN register
  Testing Rotate right, 18 bit DMAIN register
  Testing Rotate left, 18 bit DBASE register
  Testing Rotate right, 18 bit DBASE register
  Testing Rotate left, 36 bit DMAIN register
  Testing Rotate right, 36 bit DMAIN register
  Testing Rotate left, 36 bit DBASE register
  Testing Rotate right, 36 bit DBASE register
  Testing Shift left, 36 bit DMAIN register
  Testing Shift left, 36 bit DBASE register
  Testing Shift right, 36 bit DMAIN register
  Testing Shift right, 36 bit register
Testing APG error pipelines [apg_error_pipe_tb]
Testing APG data inversions [apg_data_inversions_tb]
    Checking bit1 functions
      Bit1 as Y Address Bits PASSED
      Bit1 as X Address Bits PASSED
    Checking bit2 functions
      Bit2 as Y Address Bits PASSED
      Bit2 as X Address Bits PASSED
    Checking bit1, bit2 logical combinations
      Bit1 AND Bit2 PASSED
      Bit1 OR  Bit2 PASSED
      Bit1 XOR Bit2 PASSED
    Check X and Y parity
        XYodd PASSED
        XYEven PASSED
        Xeven_Yodd PASSED
        Xodd_Yeven PASSED
        Xodd PASSED
        Xeven PASSED
        Yodd PASSED
        Yeven PASSED
    Check DTOPO inversions
      DTopo RAM PASSED
    Check Yindex Counter
      YIndex Counter PASSED
    Check Yindex Mask Inversions
          yindex plus Y, yindex = 0xffff
          yindex plus Y bar, yindex = 0xffff
          yindex plus Y, Y = 0xffff
          yindex plus Y bar, Y = 0x0000
      YIndex Mask Inversions PASSED
    Check XY Equality Functions
          xmain equal to xbase (XEQB)
          xmain less than xbase (XLTB)
          xmain less than or equal to xbase (XLEB)
          xmain equal to xfield or xbase (XEQBORF)
          ymain equal to ybase (YEQB)
          ymain less than ybase (YLTB)
          ymain less than or equal to ybase (YLEB)
          ymain equal to yfield or ybase (YEQBORF)
          xymain equal to xybase (XYEQB)
          xymain less than xybase (XYLTBXF)
          xymain less than xybase (XYLTBYF)
          xymain less than or equal to xybase (XYLEBXF)
          xymain less than or equal to xybase (XYLEBYF)
          inversion from uRAM (INVSNS)
          inversion from uDATA (XORINV)
Testing ECR X Scramble RAM - short march [ecr_xscram_short_march_tb]
Testing ECR Y Scramble RAM - short march [ecr_yscram_short_march_tb]
Testing ECR Row RAM - short march [ecr_rowram_short_march_tb]
Testing ECR Col RAM - short march [ecr_colram_short_march_tb]
Testing ECR dimm bit independence [ecr_dimm_bit_independence_tb]
Testing ECR 5N March [ecr_dimm_hw_long_march_tb]
Testing DBM DRAM - short march [dbm_dimm_short_march_tb]
```


```
Testing DBM DIMM 5N March [dbm_dimm_hw_5N_march_tb]
Testing TG Pin Scramble RAM - short march [tg_psram_short_march_tb]
Testing TG timing RAM - short march [tg_timing_ram_short_march_tb]
Testing TG SLVM RAM - short march [tg_slvm_ram_short_march_tb]
Testing TG broadcast mode [tg_broadcast_tb]
Testing TG to PE communications [tg_pe_communication_tb]
Testing PE error generation [pe_error_gen_tb]
Testing PE force drive state [pe_force_drive_state_tb]
Testing PE force drive state [pe_vz_state_tb]
Testing Pin Scramble Format RAM - short march [format_ram_short_march_tb]
Testing Pin Scramble RAM - short march [pe_psram_short_march_tb]
Testing DP ADC [adc_tb]
Testing DP PMU voltage force [pmu_vf_tb]
 Testing DP 1 PMU voltage force DACs
 Testing DP 1 PMU voltage force level accuracy
 Testing DP 2 PMU voltage force DACs
 Testing DP 2 PMU voltage force level accuracy
 Testing DP 3 PMU voltage force DACs
 Testing DP 3 PMU voltage force level accuracy
 Testing DP 4 PMU voltage force DACs
 Testing DP 4 PMU voltage force level accuracy
Testing DP PMU current force [pmu_if_tb]
 Testing DP 1 PMU current force DACs
 Testing DP 1 PMU current force level accuracy
 Testing DP 2 PMU current force DACs
 Testing DP 2 PMU current force level accuracy
 Testing DP 3 PMU current force DACs
 Testing DP 3 PMU current force level accuracy
 Testing DP 4 PMU current force DACs
 Testing DP 4 PMU current force level accuracy
Testing DP PMU voltage comparators [pmu_vcomp_tb]
 Testing DP 1 PMU comparator DACs
 Testing DP 2 PMU comparator DACs
 Testing DP 3 PMU comparator DACs
 Testing DP 4 PMU comparator DACs
 Testing DP 1 PMU comparator accuracy
 Testing DP 2 PMU comparator accuracy
 Testing DP 3 PMU comparator accuracy
 Testing DP 4 PMU comparator accuracy
Testing DP PMU voltage clamps [pmu_vclamp_tb]
Testing DP PMU current limit [pmu_ilimit_tb]
Testing DP PMU compensation capacitors [pmu_cap_tb]
Testing DP PMU/DPS current measure [range_resistor_tb]
Testing DPS voltage force [dps_vf_tb]
 Testing DP DPSn DACs
 Testing DP DPSn level accuracy
 Testing DP DPSn apg level DAC select path
 Testing DP DPSa DACs
 Testing DP DPSa level accuracy
Testing DPS switches [dps_switch_tb]
Testing DPS current share [dps_share_tb]
Testing DPS sense resistor bypass diodes [dps_diode_tb]
Testing DPS compensation capacitors [dps_cap_tb]
Testing DP DPS leakage current [dps_leakage_tb]
Testing DP DPS current capability [dps_imin_tb]
Testing DP HV voltage force [hv_vf_tb]
 Testing HV DACs
 Testing HV level accuracy
Testing DP HV leakage current [hv_leakage_tb]
Testing DP HV current measure [hv_imeas_tb]
Testing PE leakage current [pe_leakage_tb]
  Testing at  0.0 V
  Testing at  4.0 V
  Testing at  6.5 V
Testing PE VIH pin level [vih_tb]
 Testing VIH DACs
 Testing VIH level accuracy
 Testing VIH apg level DAC select path
Testing PE VIL pin level [vil_tb]
 Testing VIL DACs
 Testing VIL level accuracy
 Testing VIL apg level DAC select path
```


```
Testing PE VIHH pin level [vihh_tb]
 Testing VIHH DACs
 Testing VIHH level accuracy
 Testing VIHH apg level DAC select path
Testing PE VTT pin level [vtt_tb]
 Testing VTT DACs
Testing PE VOH pin level [voh_tb]
 Testing VOH DACs
 Testing VOH level accuracy
Testing PE VOL pin level [vol_tb]
 Testing VOL DACs
 Testing VOL level accuracy
Testing PE VZ pin level [vz_tb]
Testing PE Verniers [vern_check_tb]
Testing strobe modes [pe_strobe_mode_tb]
Testing PE XYAddr Pin Scramble [pe_ps_xy_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE XYAddr Pin Scramble [pe_ps_xy_ddr_tb]
  Testing X Address bits
    X Address 50.0MHz Test (20 ns)
  Testing Y Address bits
    Y Address 50.0MHz Test (20 ns)
Testing PE Data Pin Scramble [pe_ps_data_ddr_tb]
  Testing Data bits
    Data Bits 50.0MHz Test (20 ns)
  Testing Data Strobes
    Data Strobes 20.0MHz Test (50 ns)
Testing PE Chip Select Pin Scramble [pe_ps_cs_ddr_tb]
  Testing Chip Selects
    Chip Selects 50.0MHz Test (20 ns)
  Testing Chip Select Strobes
    Chip Select Strobes 20.0MHz Test (50 ns)
Testing PE Force Pin Scramble [pe_ps_force_ddr_tb]
  Testing Drive L/H/Z
    Drive Low  50.0MHz Test (20 ns)
    Drive High 50.0MHz Test (20 ns)
    Tri-State  50.0MHz Test (20 ns)
  Testing Strobe L/H/V/M
    Strobe Low   20.0MHz Test (50 ns)
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    Strobe High  20.0MHz Test (50 ns)
    Strobe Valid 20.0MHz Test (50 ns)
    Strobe Mid   20.0MHz Test (50 ns)
Testing PE LVM Pin Scramble [pe_ps_lvm_ddr_tb]
  Testing Drive 0/1/X
    Drive 0 50.0MHz Test (20 ns)
    Drive 1 50.0MHz Test (20 ns)
    Drive X 50.0MHz Test (20 ns) (HiZ)
  Testing Strobe L/H/V/Z
    Strobe L 20.0MHz Test (50 ns)
    Strobe H 20.0MHz Test (50 ns)
    Strobe V 20.0MHz Test (50 ns)
    Strobe Z 20.0MHz Test (50 ns)
Testing PE32 Timing Generators [pe_tg_format_tb]
  Testing NRZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing NRZ Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTO Format 5.0MHz Test (200 ns) with Window Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing RTZ Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_dclk_format_tb]
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKPOS Format 5.0MHz Test (200 ns) with Window Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Edge Strobes
  Testing DCLKNEG Format 5.0MHz Test (200 ns) with Window Strobes
Testing PE32 Timing Generators [pe_tg_mux_mode_tb]
  Testing MUX Mode 5.0MHz Test (200 ns) with Edge Strobes
  Testing MUX Mode 5.0MHz Test (200 ns) with Window Strobes
Testing VMC FIFO Resident Loop counter branching [vmc_fifo_loop_branching_tb]
         Running vmc_fifo_loop1_np_pat
         PASS: vmc_fifo_loop1_np_pat
         Running vmc_fifo_loop2_np_pat
         PASS: vmc_fifo_loop2_np_pat
         Running vmc_fifo_loop3_np_pat
         PASS: vmc_fifo_loop3_np_pat
         Running vmc_fifo_loop4_np_pat
         PASS: vmc_fifo_loop4_np_pat
         Running vmc_fifo_loop5_np_pat
         PASS: vmc_fifo_loop5_np_pat
         Running vmc_fifo_loop6_np_pat
         PASS: vmc_fifo_loop6_np_pat
Testing VMC RAM Resident Loop counter branching [vmc_ram_loop_branching_tb]
         Running vmc_ram_loop_np_pat
         PASS: vmc_ram_loop_np_pat
Testing LVM Subroutine Branching [lvm_subroutines_tb]
Testing LVM Subroutine Branching DDR [lvm_subroutines_ddr_tb]
Testing Scan Functionality [scan_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing Scan DDR Functionality [scan_ddr_tb]
  Standard Mode SCAN Tests - No Subs - No Strobes
  Standard Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
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  Standard Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Standard Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Standard Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - No Subs - No Strobes
  Split Mode SCAN Tests - No Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect == Actual
  Split Mode SCAN Tests - No Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Local Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - Remote Subs - Strobe for Expect != Actual
  Split Mode SCAN Tests - External Subs - Strobe for Expect != Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect == Actual
  TG Hold SCAN Tests - No Subs - Strobe for Expect != Actual
Testing HSB sec. connections [apg_sec_tb].
Testing ECR [ecr1_tb]
 Testing first 36 ECR data inputs with 18X, 0Y
  Testing ECR0 first 36 error lines
  Testing ECR1 first 36 error lines
Testing ECR [ecr2_tb]
 Testing last 36 ECR data inputs with 18X, 0Y
 Testing ECR0 last 36 error lines
 Testing ECR1 last 36 error lines
Testing ECR [ecr3_tb]
Testing ECR address inputs with 18X, 5Y and full speed configuration
 Testing DUT1 addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 diagonal
 Testing DUT2 addressing
  ECR1 first row
  ECR1 second row
  ECR1 third row
  ECR1 last row
  ECR1 diagonal
Testing ECR [ecr4_tb]
Testing ECR address inputs with 7X, 16Y and full speed configuration
 Testing ECR addressing
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing ECR [ecr5_tb]
Testing ECR clear with 18X, 5Y and full speed configuration
 Testing ECR0 clear
 Testing ECR1 clear
Testing ECR [ecr6_tb]
Testing ECR with 18X, 8Y and slow speed configuration
 Testing ECR addressing
  ECR0 first row
  ECR0 second row
  ECR0 third row
  ECR0 last row
  ECR0 first column
  ECR0 second column
  ECR0 third column
  ECR0 last column
  ECR0 diagonal
 Testing ECR addressing
  ECR1 first row
  ECR1 second row
```


```
  ECR1 third row
  ECR1 last row
  ECR1 first column
  ECR1 second column
  ECR1 third column
  ECR1 last column
  ECR1 diagonal
Testing DBM read widths at minimum speed configuration [dbm1_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM read speed with 32-bit data [dbm2_tb]
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM write widths at minimum speed configuration [dbm3_tb]
  32-bit width data - 18X,  8Y (pass1, loop1)
  16-bit width data - 18X,  9Y (pass1, loop2)
   8-bit width data - 18X, 10Y (pass1, loop3)
   4-bit width data - 18X, 11Y (pass1, loop4)
   2-bit width data - 18X, 12Y (pass1, loop5)
   1-bit width data - 18X, 13Y (pass1, loop6)
  32-bit width data - 10X, 16Y (pass2, loop1)
  16-bit width data - 11X, 16Y (pass2, loop2)
   8-bit width data - 12X, 16Y (pass2, loop3)
   4-bit width data - 13X, 16Y (pass2, loop4)
   2-bit width data - 14X, 16Y (pass2, loop5)
   1-bit width data - 15X, 16Y (pass2, loop6)
Testing DBM write speed with 32-bit data [dbm4_tb]
  Testing DBM write speeds with 36-bit data
  18 X,  5 Y at t_dbm_full_speed, (pass1, loop1)
  18 X,  8 Y at t_dbm_slow_speed, (pass1, loop2)
   7 X, 16 Y at t_dbm_full_speed, (pass2, loop1)
  10 X, 16 Y at t_dbm_slow_speed, (pass2, loop2)
Testing DBM [dbm5_tb]
Testing DBM write to ECR capture with full speed configuration, 18X, 5Y
 Testing DBM capture to ECR0
  DBM to ECR0 first row
  DBM to ECR0 second row
  DBM to ECR0 third row
  DBM to ECR0 last row
  DBM to ECR0 diagonal
Testing DBM [ dbm6_tb ]
Testing DBM read widths with sequential configuration, 18X, 8Y
Testing CPUI in multiple sites per controller [multisite_cpui_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_cpui_tb PASSED.
Testing APG in multiple sites per controller [multisite_apg_tb]
  Testing 2 Sites-per-Controller
  Testing 3 Sites-per-Controller
    Skipping - This site is not used in a 3 SPC configuration
  Testing 4 Sites-per-Controller
multisite_apg_tb PASSED.
SystemDiag summary [diag_summary_tb]
        Pass number : 1
        Time for this pass : 00:08:33
        Total time : 00:08:47
Final Bin: pass_bin
Done: 08/15/18 09:23:43
```


```
TestDone...bin = pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin,pass_bin

The test program is unloaded
```

Site4_1_4_V5M_Measure

V5M_Measure	Chassis_1	Slot_4						
V5M_Measure At: 08/15/18 09:15:14 On PEs: 901457 901384 901290 901466 and DPs: 929208 932536 929163 922166								
HostName	XXXXXX	HSB	819631					
Board_num	ADC_Num	AGND2DSGND	RAW	Expect	Actual	Delta	MinTol	MaxTol
Board_1	ADC_1	0	-3.668	-5.4	-3.668	1.733	-0.15	0.15
Board_1	ADC_2	0	-3.664	-5.4	-3.664	1.736	-0.15	0.15
Board_2	ADC_1	0	-3.676	-5.4	-3.676	1.725	-0.15	0.15
Board_2	ADC_2	0	-3.664	-5.4	-3.664	1.737	-0.15	0.15
Board_3	ADC_1	0	-3.676	-5.4	-3.676	1.724	-0.15	0.15
Board_3	ADC_2	0	-3.668	-5.4	-3.668	1.732	-0.15	0.15
Board_4	ADC_1	0	-3.67	-5.4	-3.67	1.731	-0.15	0.15
Board_4	ADC_2	0	-3.66	-5.4	-3.66	1.74	-0.15	0.15